AMENDMENTS TO THE SPECIFICATION

Please replace the second paragraph on page 10, beginning at line 14, with the following amended paragraph:

Fig. 1 is a simplified block diagram of an XCaliber DMS processor 101 with a higher-level subdivision of functional units than that shown in the NIO diagram of the priority document. In Fig. 1 XCaliber DMS processor 101 is shown as organized into three functional areas. An outside System Interface Unit (SIU) area 107 provides communication with outside devices, that is, external to the XCaliber processor, typically for receiving and sending packets. Inside, processor 10 1 is divided into two broad functional units, a Packet Management Unit (PMU) 103, equating to the NIO system in the priority document mentioned above, and a Stream Processor Unit (SPU) [[107]]105. The functions of the PMU include accounting for and managing all packets received and processed. The SPU is responsible for all computational tasks.

Please replace the last paragraph on page 89, beginning at line 26 and continuing to page 90, line 13, with the following amended paragraph:

Within PMU 103 there is illustrated a local packet memory (LPM) 2 19. LPM [[2191]]219 is a hardware-controlled memory implemented within PMU 103 where data packets reside before download to an output ~~networkinterface~~network interface(not shown). LPM 219 has, in a preferred embodiment, 256 KB capacity, and is made up of eight 33-KB memory cells, each having two access ports. A software-controlled external packet memory EPM 5001, external to the PMU, is provided as well, and takes any overflow from LPM 5006 in packet operations. ~~The present invention is concerned only with the LPM.~~ A register transfer unit (RTU) 5003 is illustrated herein and adapted to provide register transfer services for selecting and loading context registers (not shown) for SPU processing. A hardware controller (HC) 5004 is provided and deals with allocation status of pages in the LPM 219. A command unit (CU) 213 is illustrated within PMU 103 and adapted to receive and pass commands from SPU 105 and from SIU 107 to functional blocks within PMU 103. Conversely, command responses from the various blocks are passed back through CU 213 to SIU 107 and SPU 105. A Page Memory

Manager Unit (PMMU) 209 is illustrated and adapted to allocate virtual and atomic pages for LPM 5006.